IN THE CLAIMS:

1-42. (Previously Canceled)

43. (Currently Amended) A memory system comprising a plurality of T-RAM memory cells arranged in an array, wherein

each of the plurality of T-RAM memory cells includes a first and a second horizontal device, said first and second horizontal device being approximately the same height, each of said first and second horizontal device having a planar top surface, and

said second horizontal device includes a halo region created using a halo implant to limit a footprint of each memory cell to less than or equal to $6F^2$.

44. (Previously Amended) The memory system as in Claim 43, wherein the first horizontal device is a thyristor and the second horizontal device is a transfer gate.

45. (Currently Amended) The memory system as in claim 44, wherein the ~~transfer gate comprises a~~ halo region is of a single polarity.

46. (Previously Amended) The memory system as in Claim 45, wherein the single polarity halo region of the transfer gate is fabricated in the same steps as a halo region of the thyristor.

47-50. (Previously Canceled)

51. (Previously Amended) The memory system as in Claim 43, wherein the first device is a p-MOS device and the second device is an n-MOS device.

52. (Previously Amended) The memory system as in Claim 51, wherein the p-MOS device comprises an n-type halo region and the n-MOS device comprises a p-type halo region.

53. (Previously Amended) The memory system as in Claim 52, wherein the n-type halo region of the p-MOS device is fabricated simultaneously with fabrication steps for fabrication of a halo region of the T-RAM cells and the p-type halo region of the n-MOS device is fabricated simultaneously with fabrication steps for fabrication of a second halo region of the T-RAM cells.

54-65. (Previously Canceled)